UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,225	08/19/2003	Igor Keller	02PA053US01	6463

55497 7590 12/31/2009

VISTA IP LAW GROUP LLP
1885 Lundy Avenue
Suite 108
SAN JOSE, CA 95131

EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	PAPER NUMBER
2123	

MAIL DATE	DELIVERY MODE
12/31/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,225	KELLER, IGOR	
	Examiner	Art Unit	
	ANDRE PIERRE LOUIS	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 9/09/2009 has been received and fully considered.

2. Claims 1-41 remain pending and are presented for examination.

Response to Arguments

3. Applicant's arguments filed 9/09/2009 have been fully considered but they are not persuasive.

3.1 Applicant argues that Lee does not teach selecting timing events based at least in part upon a load of the gate, the Examiner respectfully disagrees and asserts that Lee et al. does teach the selection of at least one timing event, namely latest signal, as worst case timing event *(see Lee col.1 lines 23-27, col.7 lines 4-31),* wherein a plurality of signals containing a combination of all possible slews and arrival times and gate's characteristic taking into consideration other parameters such as capacitive loading propagated at the gates are selected *(see col.4 lines 27-43, col.5 lines 1-5, col.16 lines 8-56 and col.14 lines 25-40).* Lee clearly states that at *col.4 lines 29-33* that the signal arrival time and slew at the output are functions of other parameters such as capacitance loading and *col.5 line 1-15* show a detailed spice simulation for static CMOS gates under different slew and capacitance loading conditions.

3.2 While the applicant believes that the independent claims, along with the dependent claims should be found allowable, the examiner respectfully disagrees and asserts that the combined references cited teach the entire claimed invention, as evidenced by the grounds of rejection below.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.0 Claims 1-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent No. 6,430,731).

4.1 In considering the independent claims 1,6, 11, 19, 29, and 33, Lee et al. teaches Beakes et al. substantially teaches a computer implemented method for determining a worst-case transition, and particularly teaches the steps of determining at least a plurality of different arrival times and a plurality of different slews from a plurality of timing events propagated to an input of a gate of based at least in part upon a timing model of the gate *(col.2 lines 16-33 and col.4 line 9-col.5 line 5; also see col.7 lines 4-10)*; selecting one of the plurality of timing events propagated to the input of the gate as a worst case timing event based at least upon a load of the gate, an arrival time in the plurality of the different arrival times and a slew of the plurality of different slews of the plurality of timing events *(fig.11, col.1 lines 23-27, col.4 lines 27-43, col.5 lines 1-5, and col.6 line 31- col.7 line 31, col.14 lines 25-43 and col.15 lines 42-col.16 line 42)*; storing information related to the worst case timing event in a computer readable medium *(col.14 lines 40-43 and col.15 lines 52-62)*.

4.2 As per claims 2,7, 12, and 20, Lee et al. teaches the step of determining a plurality of gate delays for a plurality of input signals based at least in part upon the timing model of the gate *(see Lee et al. col.4 lines 27-43)*.

4.3 With regards to claims 3,8, 13, and 21, Lee et al. teaches that the step of selecting the worst-case input timing event further comprises the step of selecting a worst delay based at least in part upon the gate delays *(see Lee et al. col.15 lines 44-48)*.

4.4 Regarding claims 4,9, 14, and 22, Lee et al. teaches that the timing model comprises $To = Ti + Dg$, $Dg = F(S_I, C)$, $So = Q(S_I, C)$, where To is an output time, T_i is an input time, Dg is a gate delay, S_I is an input slew, C is a capacitive load of the gate, and So is an output slew, wherein the delay Dg of the gate depends, at least in part , on the slew of the input transition and capacitive load at the output of the gate (*see Lee et al. col.4 lines 27-43).*

4.5 Regarding claims 5,10, 15, and 23, Lee et al. teaches that the timing model is a timing library format (FTL) model (*see Lee et al. col.5 lines 7-17*).

4.6 With regards to claims 16-18, Lee et al. teaches that the output slews of the output timing events includes slew rate of the output timings, which is determined by an amount of time for a waveform to transition from a first voltage to a second voltage *(see Lee et al. col.2 lines 16-33).*

4.7 Regarding claim 24, Lee et al. teaches that the different arrival times comprise the arrival times of the timing event at each input of the gate *(see Lee et al. col.2 lines 16-33 and col.4 lines 9-43).*

4.8 As per claim 25, Lee et al. teaches that the different arrival times of the timing event at each input of the gate comprises the input times of the timing events *(see Lee et al. col.2 lines 16-33 and col.4 lines 9-43).*

4.9 With regards to claims 26,30, and 34, Lee et al. teaches that the different slews comprise transition times of the timing events through the gate *(see Lee et al. col.3 line 65-col.4 lines 43).*

4.10 Regarding claims 27,31, and 35, Lee et al. teaches that the transition times of the timing events through the gate are based at least in part upon characteristics of the gate *(see Lee et al. col.3 line 65-col.4 lines 43).*

4.11 As per claims 28,32, and 36, Lee et al. teaches that a duration of the transition times of the timing events through the gate is based at least in part upon characteristics of the gate *(see Lee et al. col.3 line 65-col.4 lines 43).*

4.12 With regards to claims 37-41, Lee et al. teaches that information related to the worst-case timing event is stored in a memory *(see Lee et al. col.14 lines 40-43 and col.15 lines 52-62).*

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5.1 Hampel et al. (U.S. PGPUB No. 2003/0131160) teaches a timing calibration apparatus and method for a memory device signaling system.

6. Claims 1-41 are rejected and **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. P. L./
Examiner, Art Unit 2123

December 29, 2009

/Paul L Rodriguez/

Supervisory Patent Examiner, Art Unit 2123